"COMPUTERIZED ANALOG/DIGITAL INPUT/OUTPUT UNIVERSAL SYSTEM"

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КОМПЬЮТЕРИЙН УДИРДЛАГАТАЙ АНАЛОГ БА ЦИФРЭН СИГНАЛЫН ОРОЛТ/ГАРАЛТЫН УНИВЕРСАЛЬ СИСТЕМ

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Аналог оролттой, цифрэн гаралттай, зэрэгцээ болон цуваа хэлбэрийн цифрэн сигналыг хоёр чиглэлд дамжуулах боломжтойгоос гадна орчин үеийн персональ компьютертай холбогдон ажиллах универсаль системийг зохион бүтээв. Олон дахин программчлагддаг "GAL" микросхемийг ашиглаж системийн блокуудын овор хэмжээг багасгаснаас гадна дурын программчлалын хэл ашиглаж компьютераас бүрэн удирдаж болох онцлогтой. Системийн ерөнхий бүтэц, ажиллах зарчмыг тусгав.

GENERAL DESCRIPTION

Figure 1 shows basic connections of the Computerized analog/digital inpit/output Universal System (CUS). This system consists from:

- Analog/Digital and Input/Output device (A/D&I/O)
- 16-bit PC slot buffer card (PC-SB)
- Personal computer (PC)

By connecting the A/D&I/O device to the computer the system becomes more universal, flexible and programmable from the PC for other different purposes. The system can be programmed using any programming language, like Pascal, GW or Quick or Visual Basic, Assembler, C or C+ or Visual C, Delphi etc. in the DOS and Windows environments. All running measurements and status of controlling procedures can be simultaneously shown on the computer screen user-friendly depending on user's desire.

We need to use fast, multi-input Analog to Digital Converter (ADC) to receive simultaneously a number of analog signals from several kinds of detectors, sensors and transducers which control some technological procedure and environmental condition. ADC converts analog signal into digital form and these converted signals are transferred to the PC which processes only digital data.

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During the designing period, we have decided to add to ADC device the following so that it becomes more universal, flexible, easy to program and can be used in industrial, scientific and educational areas without any hardware and software problem:

- Digital to Analog Converter (DAC)
- Three serial input and output ports
- Three parallel bi-directional ports

A/D&I/O device is always under control from PC. Data, addresses and control signals of it are transferred bi-directionally to and from PC through the PC-SB card. Then a specially developed software in PC will process received data from the A/D&I/O device accordingly by methodology.

ANALOG/DIGITAL INPUT/OUTPUT DEVICE

Figure 2 shows an electronic circuit schematic drawing of the device in more detail. It has the following inputs and outputs:

a. Eight analog inputs of the ADC. There is a possibility to receive simultaneously maximum eight different analog signals from detectors, sensors and transducers.
b. Two digital outputs of the DAC. Using them it is possible to control some analog devices from the computer. For example: movement of different types of electro-motors; audio, video and alarm systems, some mechanical actions and exact positioning of some parts in a controlling area.
c. Three serial and three parallel digital inputs and outputs. Using them it is possible to send and receive digital signals in parallel or in serial forms and to control some digital devices, like stepper motors, security systems, transmission of digital signals to an another computer, equipment and some other peripheral devices.
d. 16-bit bi-directional data bus. Using this we can transmit simultaneously 16-bit digital data to and from the PC to control each and every input and output of the A/D&I/O device individually and simultaneously on the PC monitor.

MPC508AP TYPE MULTIPLEXER

Analog inputs of the CUS are connected to the ADC through MPC508AP type multiplexer. It is an analog and eight channel chip with the active overvoltage protection. Analog input levels may greatly exceed it's own power supply without damaging the device and channels are independent from each other, so that there is no disturbing problem of a particular signal or channel to other channels. Analog inputs can withstand constant 70V peak-to-peak levels and typically survive static discharges beyond 4000V. Signal sources are protected from short circuiting. Each input presents 1K of resistance under a condition that multiplexer supply loss should occur if there is a short circuit.

These features make this device ideal for use in a system where the analog inputs originate from external equipment or separately powered circuitry. Therefore we have chosen this device to use in our system. It includes an array of eight analog switches, a

digital decode circuit for channel selection, a voltage reference for logic threshold and an enable input for device selection when several multiplexers are present. Switches are guaranteed to "break-before-make", so that two channels are never shorted together.

GENERAL ARRAY LOGIC

General Array Logic (GAL) is a new technology in the IC manufacturing field. With complete logic source GAL is today committed to serving the market with high volume families and introducing Programmable Logic Device (PLD) which show one of the fastest growth rates in the semiconductor market. It is ideal for simplifying the design process, because the designer can implement the exact logic function whenever and wherever required. Programmable logic offers more efficient utilization, as well as reduced chip count, by simplifying the lay-out process at both conceptual and implementation stages. GAL's are ideal devices among PLD's for following reasons:

- GAL devices are fabricated using modern technology of very high speed Electrically Erasable CMOS (EE-CMOS) technology which offers the highest degree of testability and quality of any process technology.
- In fact functionality can be 100% tested and that guarantees 100% programming and functional yield to the customer with no further board rework. Therefore GAL's are ideal for prototyping and for unforecasted design changes.
- The Electrically Erasable Cell Technology allows reconfigurable logic, reprogrammable cells and guaranteed 100% yields. The high speed CMOS technology allows to use a low power (90/70mA maximum Active/Standby-in half power and 45/35mA maximum Active/Standby-in quarter power) and high speed (15 to 25ns maximum access-in half power and 20 to 35ns maximum access-in quarter power).
- Their speeds are as fast as any other bipolar programmable logic devices except ECL, but they have the low power consumption of CMOS.
- GAL devices utilize the reprogrammable Output Logic Macrocell (OLMC) which allows the user to configure outputs as needed and to replace several other programmable logic devices and low density gate arrays.
- Data retention of the GAL exceeds 20 years and there is preload and power-on reset of all registers.
- There are a security cell which prevents copying logic and a possibility of high speed programming algorithm.

The main advantages of GAL devices come from their intrinsic "genericity" that allows the user to define the architecture and functionality of each output and also has advantages at the shop floor level: users can put in inventory one generic GAL type instead of many different PAL devices types; this will not only saves money, but also minimizes the paper work and reduce manufacturing flow. For instance, one GAL16V8 type device can replace 21 different bipolar PAL devices. There are several types of GAL chips depending on programming voltage level and number of inputs and outputs. For example: GAL16V8, GAL20V8, GAL18Z8, GAL39V18.

During the designing period of the system, we have decided to use GAL16V8 type chip to save space in the Printed Circuit Board (PCB) and to assemble the A/D&I/O device only on one double-side and euro-standard size PCB.

The programmable memory technology of this device applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels. The 20-pin GAL16V8 features eight programmable outputs allowing each output to be configured by the user. Programming is accomplished using special hardware and software tools. We can do maximum 100 erase/write cycles in the one GAL device. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

In the case of the developing system, two GAL16V8 type chips have been used, because we want to control more that 16 inputs. It has 20 pins and assembled in a plastic DIP package. 16V8 means that there are maximum 16 possible inputs and 8 outputs. If we use all 8 outputs, the maximum number of inputs becomes 9 and there are left 3 pins for the IO/CLK (Input and Output Clock signal), GND (Ground) and a Power Supply Voltage. 7 outputs from 9 are bi-directional, thus these 7 outputs can be programmed as inputs and maximum number of inputs becomes 16.

Two logic programs for the GAL16V8 have been developed to control the address decoder logic operations of the ADC, DAC and bi-directional serial and parallel ports of the PC A/D&I/O device.

ADS774 TYPE ANALOG TO DIGITAL CONVERTER

The Burr-Brown ADS774 type modern integral circuit was selected as an ADC in the CUS. This is a 12-bit successive approximation Analog-to-Digital Converter using an innovative capacitor array implemented in low-power CMOS technology. It has internal sampling, low power consumption (maximum 120mW) and the ability to operate from a single +5V supply. The ADS774 is complete with internal clock, micro-processor interface, three-state outputs and internal scaling resistors for input ranges of 0V to −10V, 0V to +20V, +/-5V and +/-10V. The maximum throughput time is 8.5us over the full operating temperature range including both acquisition and conversion. Complete user control over the internal sampling function facilitates elimination of external sample hold amplifiers in most existing designs. The ADS774 can be easily interfaced to most microprocessor and computer-controlled systems. The microprocessor and personal computer may take full control of each conversion or the converter may operate in stand-alone mode controlled only by the R/C input of it. Full control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion and reading the output data when ready the choosing either 12 bits all at once, or 8 most significant bits (MSB) followed by the 4 least significant bits (LSB) in a left-justified format.

In our design we have chosen 12-bit conversion cycle to get more exact information from the detectors, sensors and transducers. The control inputs of the ADC are all with the transistor-transistor logic (TTL) and Complementary Metal-Oxide Semi-

conductor (CMOS) devices compatible and easy to use. The ADS774 offers four standard input ranges. In the case of developing system, we have chosen 10V input range. This range is suitable for wide-used transdusers and sensors. Therefore we have used only the pin#13 (10V-IN) and the pin#14 (20V-IN) is connected to the analog ground. Each range has necessary connections along with the optional gain and offset trim circuits. The Bipolar Offset (pin#12) is connected either to analog common (J1) for operation, or to 2.5V reference output (J2) for bi-polar operation. In the developing design circuit we have used jumper switches to this input to have both possibilities.

The ADC input 10V-IN (pin#13) is connected to the analog inputs of the system through an "OP27" type operational amplifier and an "HA3621A0520" type electronic-relay (K1) with a 220 Ohm potentiometer (P1). The electronic-relay is used to switch automatically the amplified analog signals from the range of +/-5V to +/-10V according to the amplitude of the receiving analog signals from the detectors, sensors or transducers.

The five control lines of the ADC, namely CS, AO, R/C, CE and STS, are connected to the GAL devices and 12-bit output bus of it is connected to the PC through PC-SB card.

8012 TYPE D/A CONVERTER

Two pieces of DAC8012 type, CMOS, 12-bit multiplying Digital to Analog Converter (DAC) with memory are used in the A/D&I/O device to make it more universal and programmable. The DAC has on-board, fast and TTL/CMOS compatible data latches and three-state TTL/CMOS compatible output buffers that feature "memory" read-write operation. Data is loaded into the latches by a single 12-bit wide word and can be read back on the same data lines. The DAC8012 can be directly connected to the 12-bit or 16-bit bus. The read back function makes the DAC8012 particularly well-suited for applications in automatic test equipment, industrial automation and other multi-channel micro-processor or computer controlled systems that require keeping track of the current DAC output data without using an extra memory location for each channel.

Low power dissipation and single-supply operation from +5V to +15V makes the DAC8012 an excellent choice in low-power remote and digital controller systems with a large number of analog outputs. Four-quadrant multiplying capability and 12-bits linearity allows the DAC to be used in low-noise, wide-bandwidth, low-distortion, digitally-controlled precision attenuator, filter and other applications. The DAC8012 gives maximum of 4V amplitude analog output signal. In the developing system this output signal amplified up to 15V for further applications. The GAL16V8 devices control these DAC8012 chips under supervision from the connected PC into the system.

BI-DIRECTIONAL SERIAL AND PARALLEL PORTS

The M5L8255AP-5 type parallel port chip, D8253C-2 type down counter are used as parallel and serial ports respectively in the A/D&I/O device. The 8255 chip has three

independent, eight-bit parallel ports: port_A, port_B and port_C. The 8253 chip has three independent, eight-bit down counters or serial ports: counter_0, counter_1 and counter_2.

Each port and counter can be programmed from the PC completely separately from each other for different purposes. The GAL16V8 devices control chip selection operations of these ports and counters. All the inputs and outputs of the ADC, DAC, serial and parallel ports are mounted on the front panel of the A/D&I/O device using 9-pin and 25-pin connectors. Figure 3 shows the internal separate parts of the "PC A/D&I/O" device with the corresponding hardware addresses and with the exact input/output pin numbers. Figure 4 shows more in detail every hardware fixed input and output addresses of the each port, counter, Least Significant Byte (LSB) and Most Significant Byte (MSB) of the ADC and DAC devices. It also shows output addresses of the 8255 type parallel port control register, 8253 type down counter status resister and channel select, start conversion and sensitivity addresses of the ADC.

16 BIT PC SLOT BUFFER CARD

Figure 3 shows basic connections of the PC-SB to the 16-bit PC data bus. This is a special card designed for 16-bit IBM type PC data bus. From the point of the PC hardware protection view, it is very important device. Its main purposes are:

a. This card works like a safety fuse for the Integral Circuits of the PC motherboard. If a short circuit or a dangerous hardware accident will occur inside the developing system, which is connected to the PC, this card will protect the most expensive PC hardware parts from a possible break-down problem.
b. The fixed hardware addresses from 300H to 31FH are left in any modern PC hardware architecture for a future hardware and software design. This new PC-SB card enables to use only these reserved addresses of the PC by an external system which can be connected to it. By writing a program using any language on the PC, it is possible to enable and disable one or some of these addresses for a particular use independently from each other.
c. Thus every and each address of this range can be used separately without address overlapping problem when the developing industrial system is receiving simultaneously eight analog signals or when some other software programs (DOS, UNIX and WINDOWS systems or any other common application software) are running on the computer which is connected to the system.
d. This device works as a buffer or temporary storage unit for the digital signals which should be transferred and processed further by the PC. It can receive 8-bit digital signals from the system parallelly and buffer or store them for a while until the next 8 bits are completely received into its memory. Then this parallel 16-bit digital signal is transferred parallelly into the computer's memory for a further processing by a specially developed program. It makes the running time of the signal processing procedure shorter and fast.
e. Also the device can receive the digital signal in serial form, bit by bit and buffer them until they form 16-bit parallel digital signal. Then the PC receives those parallel signals simultaneously into memory for further processing.

From the above mentioned features we called this device as a "16-bit PC slot buffer card". It is very useful card especially during the hardware designing and testing period of the system. It protects the expensive PC from an emergency hardware problem which can occur any time inside and outside of the system during the experimental and utilization periods. Using this computer card and having parallel 16-bit digital data and exact addresses for every and each input and output, there must be no problem to write an user-friendly program on the PC for processing the received data from the system.

Figure 4 shows an electronic circuit schematic drawing of the "16-bit PC slot buffer card" in more detail. It consists of an address decoder and a 16-bit three-state buffer. In this circuit design we have taken the following five ranges of the PC hardware addresses:

- First eight-address range from 300H to 307H, where
  300H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0000_0000B and
  307H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0000_0111B
- Second eight-address range from 308H to 30FH, where
  308H = A9A8_A7A6A5A4_ A3A2A1A0 = 11_0000_1000B and
  30FH = A9A8_A7A6A5A4_A3A2A1A0 = 11_0000_1111B
- Third eight-address range from 310H to 317H, where
  310H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0001_0000B and
  317H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0001_0111B
- Fourth eight-address range from 318H to 31FH, where
  318H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0001_1000B and
  31FH = A9A8_A7A6A5A4_A3A2A1A0 = 11_0001_1111B
- Fifth address range or "all 16-address range " from 300H to 31FH, where
  300H = A9A8_A7A6A5A4_A3A2A1A0 = 11_0000_0000B and
  31FH = A9A8_A7A6A5A4_A3A2A1A0 = 11_0001_1111B

where "H" means an hex-decimal counting system and "B" means a binary counting system.

In general, from the above binary address distributions, the address bits A9A8_A7A6A5A4_A3A2A1A0 should be equal to 11_000X_XXXX, where "X" means it can be neither logic "1" nor "0". Therefore the bits A9 and A8 must be always logic "1", and A7, A6 and A5 must be always logic "0". Other address bits might be neither "1" nor "0". Considering these conditions we have designed a small logic trick using the 74LS138 and 74LS00 to work only in the above mentioned address ranges. The computer control signals IOWR (Input and Output WRite), IORD (Input and Output ReaD), IRQ3 (Interrupt ReQuest #3) and IRQ5 (Interrupt ReQuest#5) are buffered together with the addresses bits and data signals in the 74LS245 type three-state integral circuits.

Using this card we can buffer 10-bit address signals from A0 to A9, 16 bit data signal from D0 to D15 and the control signals IOWR, IORD, IRQ3 and IRQ5 for further use by the system.

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